Illini Senior Kingfishers

Michael Gulson

Nathan Sparacino

Hyojung Kwon

Roadmap cp1

For checkpoint 2 we must improve upon our cp1 datapath to handle all basic RV32I instructions, implement a data cache and instruction cache, implement an arbiter, and connect shadow memory. Our group has found that working together as much as possible is useful to keep everyone on the same page and to ensure smooth debugging and testing. For this reason, we will all work together in designing the L1 caches with Nikki taking the lead. Nikki will also design the arbiter. Nathan and Michael will make sure our pipeline can handle all basic RV32I instructions. Michael will connect the shadow memory with the help of Nathan. Verification will be done together. We found it helpful to be on Zoom during debugging and verification to ensure everyone is on the same page. Though we will try to debug and do verification together as much as possible, the one who implemented a design will be most useful in debugging and verification of that design. We suspect that we may encounter troubles with integrating all our design elements for CP2. For this reason, it is important that design with attention to detail and verify each component before we test the design altogether. This should help us mitigate some troubles in verifying the entire design. We plan to start early to leave ample time for verification and debugging.